IEEE 2013 VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS

1.A Built-In Repair Analyzer With Optimal Repair Rate for Word-Oriented Memories.

2.A High Speed Low Power CAM With a Parity Bit and Power-Gated ML Sensing.

3.A Wide-Range PLL Using Self-HealingPrescaler/VCO in 65-nm CMOS.

4.BComputing Two-Pattern Test Cubes for Transition Path Delay Faults.

5.Design and Implementation of an On-Chip Permutation Network for Multiprocessor System-On-Chip.

6.Effective and Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flops.

7.FPGA Implementation of FFT Algorithm for IEEE 802.16e (Mobile WiMAX)

8.Low-Complexity Multiplier for GF(2m)Based on All-One Polynomials.

9.Modeling Spectral Envelopes Using Restricted Boltzmann Machines and Deep Belief Networks for Statistical Parametric Speech Synthesis.

10.Secure Dual-Core Cryptoprocessor for Pairings Over Barreto-Naehrig Curves on FPGA Platform.

11.VLSI Architecture of Arithmetic Coder Used in SPIHT.

12.A High Performance Video Transform Engine by Using Space Time Scheduling Strategy.

13.A Low-Complexity Turbo Decoder Architecture for Energy-Efficient Wireless Sensor Networks.

14.An Energy-Efficient L2 Cache Architecture Using Way Tag Information Under Write-Through Policy Constant Delay Logic Style

15.Constant Delay Logic Style

16.Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool.

17.Effective and Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flops.

18.Glitch-Free NAND-Based Digitally Controlled Delay-Lines

19.Low Latency Systolic Montgomery Multiplier for GF(2m) Finite Field Based on Pentanomials.

20.Pipelined Parallel FFT Architectures via Folding Transformation

21.Techniques for Compensating Memory Errors in JPEG2000

22.A High Speed Low Power CAM With a Parity Bit and Power-Gated ML Sensing.

23.A Unified Graphics and Vision Processor With a 0.89 W/fps Pose Estimation Engine for Augmented Reality.

24.Built-In Generation of Functional Broadside TestsUsing a Fixed Hardware Structure.

25.CORDIC Designs for Fixed Angle of Rotation

26.DS-CDMA Implementation With Iterative Multiple Access Interference Cancellation.

27.Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes.

28.High-Speed Low-Power Viterbi Decoder Design for TCM Decoders

29.Low-Cost FIR Filter Designs Based on Faithfully Rounded Truncated Multiple Constant Multiplication/Accumulation.

30.Pipelined Radix- Feedforward FFT Architectures

31.Thermal-Constrained Task Allocation for Interconnect Energy Reduction in 3-D Homogeneous MPSoCs.