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# VLSI - IEEE 2015 - 2016 Projects

1. A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter For Sub-mW Energy Harvesting Applications

2. A Generalization Of Addition Chains And Fast Inversions In Binary Fields

3. A Generalized Algorithm And Reconfigurable Architecture For Efficient And Scalable Orthogonal Approximation Of Dct

4. A Low Complexity Scaling Method For The Lanczos Kernel In Fixed-Point Arithmetic

5. A Multicycle Test Set Based On A Two-Cycle Test Set With Constant Primary Input Vectors

6. A Self-Powered High-Efficiency Rectifier With Automatic Resetting Of Transducer Capacitance In Piezoelectric Energy Harvesting Systems

7. A Synergetic Use Of Bloom Filters For Error Detection And Correction

8. Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic

9. Algorithm And Architecture For A Low-Power Content-Addressable Memory Based On Sparse Clustered Networks

10. An Efficient Constant Multiplier Architecture Based On Vertical-Horizontal Binary Common Sub-Expression Elimination Algorithm For Reconfigurable Fir Filter Synthesis

11. Comments On "Low-Latency Digit-Serial Systolic Double Basis Multiplier Over GF (2m ) Using Subquadrat Ic Toeplitz Matrix- Vector Product Approach"

12. Communication Optimization Of Iterative Sparse Matrix - Vector Multiply On GPUs And FPGAs

13. Efficient Coding Schemes For Fault-Tolerant Parallel Filters

14. Efficient Sub Quadratic Space Complexity Architectures For Parallel Mpb Single- And 16. For All Trinomials Using Toeplitz Matrix-Vector Product Decomposition

15. Fast Sign Detection Algorithm For The Rns Moduli Set {2n+1 - 1, 2n - 1, 2n}

16. Fault Tolerant Parallel Filters Based On Error Correction Codes

17. Fine-Grained Critical Path Analysis And Optimization For Area-Time Efficient Realization Of Multiple Constant Multiplications

18. Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic

19. Fully Reused VLSI Architecture Of Fm0/Manchester Encoding Using Sols Technique For DSRC Applications

20. High - Throughput Finite Field Multipliers Using Redundant Basis For Fpga And Asic Implementations

21. Low Delay Single Symbol Error Correction Codes Based On Reed Solomon Codes

22. Low-Complexity Tree Architecture For Finding The First Two Minima

23. Low-Latency High-Throughput Systolic Multipliers Over For Nist Recommended Pentanomials

24. Low-Power And Area-Efficient Shift Register Using Pulsed Latches

25. Low-Power Programmable PRPG With Test Compression Capabilities

26. Mixing Drivers In Clock-Tree For Power Supply Noise Reduction

27. New Regular Radix-8 Scheme For Elliptic Curve Scalar Multiplication Without Pre-Computation

28. Novel Block-Formulation And Area-Delay - Efficient Reconfigurable Interpolation Filter Architecture Formulti - Standard SDR Applications

29. Novel Shared Multiplier Scheduling Scheme For Area-Efficient FFT/IFFT Processors

30. Obfuscating DSP Circuits Via High-Level Transformations

31. One Minimum Only Trellis Decoder For Non – Binary Low - Density Parity - Check Codes

32. Partially Parallel Encoder Architecture For Long Polar Codes

33. Piecewise-Functional Broadside Tests Based On Reachable States

34. Pre-Encoded Multipliers Based On Non-Redundant Radix-4 Signed-Digit Encoding

35. Recursive Approach To The Design Of A Parallel Self-Timed Adder

36. Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block

37. Scan Test Bandwidth Management For Ultralarge-Scale System-On-Chip Architectures

38. Simplified Trellis Min–Max Decoder Architecture For Nonbinary Low-Density Parity-Check Codes

39. Skewed-Load Test Cubes Based On Functional Broadside Tests For A Low-Power Test Set

40. VLSI Computational Architectures For The Arithmetic Cosine Transform