International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 12, December-2015

A New Topology for Asymmetrical Multilevel Inverter

A Cascaded Multilevl Inverter with Reduced Number of Switches

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***Abstract*— The main objective of this paper is to design of new asymmetrical multilevel inverter topologies with reduced number of switches. This will give an efficient way of producing multistep waveform with reduced harmonics.**

***Keywords*— Multilevel Inverter; Topologies;Harmonics;Power System; Efficiency**

I. INTRODUCTION

Today demand of electrical power is increasing to a great extent. So to meet the requirements, generation of power is also increases. This can be achieved by storing the power through batteries in the form of D.C and this stored energy can be utilized by converting into A.C power with the help of "INVERTER". The multilevel inverter have become more popular over the years in electric high power applications with the promise of less disturbances, possibility to function at lower number of switches and switching frequencies. In addition the advantage of multi level inverter is, it can also be use renewable energy resources.

In multilevel inverter, output level occurred in a proper way so as to achieve the approximated sinusoidal wave. If these levels are more, then their stair case waveform is closed to sinusoidal waveform. For getting more levels various topologies are proposed, but the number of levels achieved is limited to circuit complexity as well as cost of equipment. That is why this paper is focused on making circuit simple as much as possible with less number of switching devices.

In this paper a new multilevel inverter topology is introduced and analyzed. This is a cascaded asymmetrical multilevel inverter with reduced number of switches.

II. BASIC COCEPT OF MULTILEVEL INVERTER

Conventional two level inverter is mostly used today to generate an A.C voltage from D.C voltage. The two level inverter can only create two different output voltages for the load, $V_{dc}/2$ or $V_{dc}/2$ (when inverter is fed with V_{dc}) as shown in figure1. To build up an AC output voltage these two voltages are usually switched with PWM as shown in figure 2.

The concepts of multilevel inverter do not depend on just two levels of voltage to create on AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother.

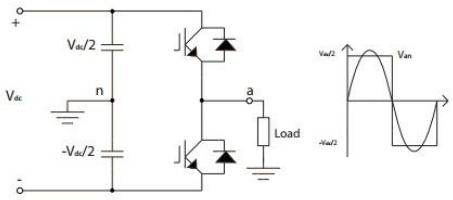

Fig. 1. Basic two level inverter

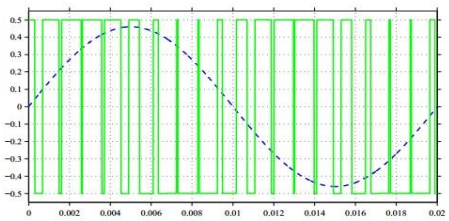

Fig.2. PWM modulation

III . PROPOSED TOPOLOGY FOR MULTILEVEL INVERTER

The main objective of this proposed topology is to design the multi level inverter with reduced number of switches and voltage sources. The output voltage can be obtained with less distortion and losses and as smooth as possible in the form of pure sinusoidal waveform.

The following figure gives the representation of proposed topology as a basic cell configuration.

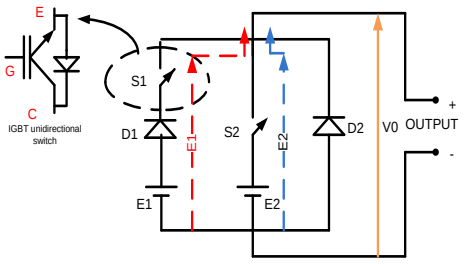

Fig.3. basic unit cell for proposed topology

This basic cell consists of Two unidirectional IGBT switches and two diodes and two DC sources E1 and E2 (E2>E1). Proposed basic cell can produce two output voltage levels across the load connected. When the switch S1 is turned ON

then the output voltage across the load is E1 Volts. Then if switch S2 is triggered by the gate signal the output voltage V0 across the load is E2 Volts by keeping the other switch is in OFF mode.

STATE	S1	S2	OUTPUT (V0)
1	ON	OFF	E1
2	OFF	ON	E2

Table1. Switching sequence f the cell

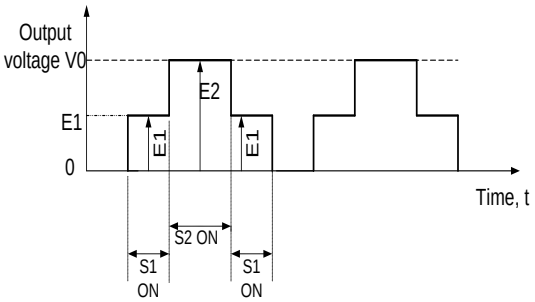

Fig.4. output voltage waveform of cell

IV. PROPOSED TOPOLOGY FOR 5- LEVEL

The basic proposed asymmetric multilevel inverter (AMLI) for generating five level AC stepped voltage waveform across the load is as shown in the figure. In the circuit, the requirements of switches and voltage sources as: two voltage sources of E1, E2= 2E1, two switches of unidirectional type S1,S2, a H-Bridge consists of 4 unidirectional switches such as T1,T2,T3,T4 and two diodes as D1,D2. Here unidirectional switch can be IGBT (Insulated Gate Bipolar Transistor) with anti-parallel diode mainly used for medium power applications. Two possible voltage levels can be generated as E1and 2E1 by switches S1 and S2 turned on with respectively as well as negative levels are also possible by use of H- Bridge, such as –(E1) , - (2E1).

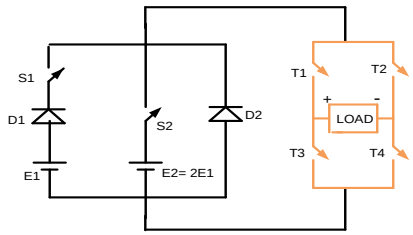

Fig.5. asymmetrical multilevel inverter for 5-Level output

For production of 5-level output for basic proposed topology, proper switching sequence is required as in TABLE 3. For level E1, switches S1,D1,T1,T4 are turned ON and at this instant the diode D2 is in reverse bias as E1 voltage makes the this diode reverse bias. For level E2=2E1, switches used are S2, T1, T4. At this instant also diode D2 is also reverse bias. For negative voltage values in the output, just by switching ON by S2, S3 and turn OFF of S1, S4 in H-bridge with combination switching sequence of positive voltage values as shown in table 3.

V0	Step	S1	S2	D1	D2	T1	T2	T3	T4
0	1	0	0	0	0	1	1	0	0
						0	0	1	1
E1	2	1	0	1	0	1	0	0	1
2E1	3	0	1	0	0				
-E1	4	1	0	1	0	0	1	1	0
-2E1	5	0	1	0	0				

Table 3: switching sequence for basic 5-Level MLI

The table 3 represents the five different values of output waveform with values 0, E1, 2E1, -E1, -2E1 and ‘1’ represents ON state and ‘0’ represents OFF state. The peak voltage across the load is 2E1.

V. THE GENERALIZED FORMAT OF MLI

The general circuit for obtaining different levels of output waveform with reduced number of switches can be possible through this topology. Hence analysis of this topology can be done.

A. General circuit diagram for definite no. of levels

The following fig.6 represents the cascaded connection of basic cell topologies so as to produce the definite no. of levels.

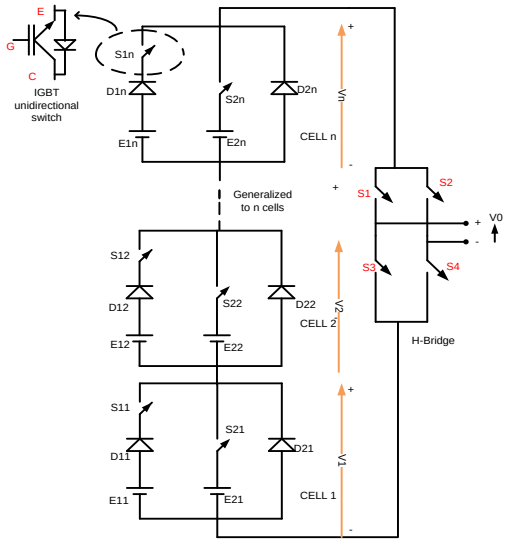

Fig.6. generalized format of developed cascaded multilevel inverter topology

In this extended proposed topology, ‘n’ no. of basic cells is connected in series to produce multilevel output ‘V0’. This output is sum of individual cell output voltages. The following is the expression form,

$$V_0 = \sum_{i=1,2\ldots n} V_i$$

In the above equation V1, V2,…Vn are individual output voltages across cell1, cell2,..cell n. proper switching ON and OFF of the switches required output can be obtained.

B. Algorithm used for voltage calculation

Third proposed method for calculating the values of voltage sources is as shown in the below. In this method asymmetry of voltage sources is more. It is important to note that if asymmetry increases the complexity and cost of inverter equipment is also increases, but the steps in output waveform are increases for same no. of switches used in second method. The following analysis is made to calculate the voltage values, no. of switches required for the extension of 'n' no. of cell connected in cascaded form. In other words, the mathematical form is as shown in below fig12. Now, in this method the voltage source values are not equal, this topology is suitable for PV cell arrays. To exemplify the operation of algorithm , a case study has given as 17-level inverter.

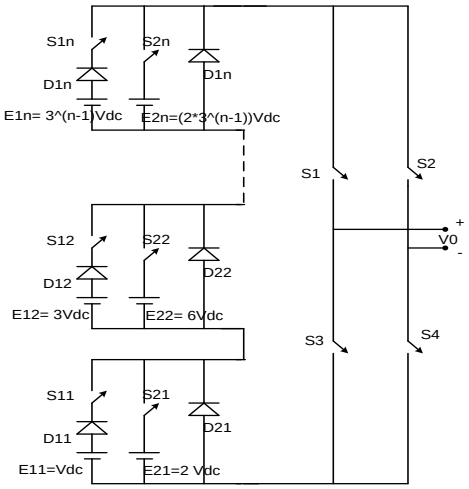

Fig.7. Asymmetrical cell voltage configuration for developed topology

voltage source values is as,

In CELL-1, E11=Vdc, E21= 2Vdc

CELL-2, E12=3Vdc, E22= 6Vdc

CELL-3, E13= 9Vdc, E23=18Vdc

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CELL-n, E1n = $3^{n-1}.V_{dc}$, E2n= $2.3^{n-1}.V_{dc}$

Now, in this method the voltage source values are not equal, this topology is suitable for PV cell sources.

Number of voltage levels, N levels = $2.3^n - 1$
Number of IGBT switches, N switches = $2n+4$
Number of voltage sources, N sources = $2n$
Variety of voltage sources, N asymmetry =$2n$
Number of diodes ,N diode = $2n$

Level	S11	S21	S12	S22	D11	D21	D12	D22	T1	T2	T3	T4
8	0	1	0	1	0	0	0	0	1	0	0	1
7	1	0	0	1	1	0	0	0				
6	0	0	0	1	0	1	0	0				
. .												
1	1	0	0	0	1	0	0	1				
0	0	0	0	0	0	0	0	0	1	1	0	0
									0	0	1	1
-1	1	0	0	0	1	0	0	1	0	1	1	0
. .												
-6	0	0	0	1	0	1	0	0				
-7	1	0	0	1	1	0	0	0				
-8	0	1	0	1	0	0	0	0				

Table 4: switching sequence for 17-level inverter

VI. CONCLUSION

In this paper an asymmetrical cascaded multilevel inverter is proposed. This algorithm is applied for getting a 17-level inverter with less number of IGBT's which is very much advantageous as compared to pre-existing topologies. The proposed topology is advantage as compared to existing topologies in terms of number of switches, number of diodes, and number of sources with number of levels generated. The 17-level cascaded multilevel inverter is gives good results in terms of percentage of THD.

VII. REFRENCES

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